Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to add antecedent basis as suggested by Examiner and to correct grammatical errors.

The claims have been amended to correct grammatical errors and dependencies to over com Examiners objection/rejections and more clearly claim Applicants invention.

Support for the amended claims is found in the original claims. No new matter has been added.

For example support for the amendments is found in paragraph 0027:

"Referring to Figure 2C, in another embodiment, a plurality of trench filling layers are formed with one or more CVD USG

layers, e.g., SACVD, APCVD, or HDPCVD, together with one or more SOG layers, with an optional annealing process performed between each layer deposition, but at least following deposition of the uppermost trench filling layer. For example, a first layer 28A of CVD USG or SOG (including a curing process) is deposited to about less than about 1/2, e.g., about 1/3 the depth of the trench by a first deposition using a CVD process or SOG process (including a curing process) followed by an annealing process according to preferred embodiments. A second layer 28B of CVD USG or SOG (including a curing process) is then deposited to about the same thickness followed by a second annealing process. A third layer e.g., 28C of CVD USG or SOG (including a curing process) is then deposited to a final thickness e.g., the deposited layers having a total thickness of from about 2000 to about 8000 Angstroms, followed by a third annealing process. Preferably, a HDP-CVD process is used for only the second and subsequent deposited layers e.g., 28B, 28C layers following initial depositions e.g., first and second layers of SOG or APCVD or SACVD, to reduce the possibility of void formation. In addition, with multiple layers being formed of SOG oxide, SACVD

oxide (USG) and/or APCVD oxide (USG), an annealing process between layer depositions may be optionally foregone, the annealing process be carried out following deposition of the final oxide layer.

Claim Rejections under 35 USC 112

Claims 1, 6, 13, 14, 15, claims 8-11, and claims 17-31 have been amended to overcome Examiners rejection.

Claim Rejections under 35 USC 102

1. Claims 1-6, 12, 14-19, and 28 stand rejected under 35 USC 102(b) as being anticipated by Ishitsuka et al. (US 6,242,323).

Ishitsuka discloses an STI structure and a method for forming the same to form an isolation structure with a desired radius of curvature in an upper edge portion of the trench (groove) see Abstract) and reducing stress generation around the upper end of the trench (groove)(see col 2, lines 58-61) as well

as reducing stresses generated due to sintering of an embedded silicon oxide film (see col 2, lines 66- col 3, line 3).

In one embodiment, a silicon nitride film is formed on the inside boundary of the trench and semiconductor substrate underneath a silicon oxidation liner (lining the trench) by nitriding and annealing (see e.g., col 7, lines 40-46). In another embodiment a silicon nitride film is formed by CVD over the silicon oxidation liner prior to depositing a silicon oxide filling layer (see e.g., col 5, lines 5-8; lines 59-61). Ishitsuka discloses that the silicon oxide film is formed by a "CVD, sputtering etc." which "are usually porous films" but does not disclose a particular type of CVD process or the type of silicon oxide (see e.g., col 15, lines 11-18). Ishitsuka discloses that the silicon oxide film is then annealed to "make the film compact" (see col 15, lines 20-23) and lessen stress caused by forming the oxidized silicon liner (col 18, lines 31-60) around the upper edge of the trench (groove).

In all embodiments, Ishitsuka discloses forming either a

single trench filling layer (CVD silicon oxide), or forming an intermediate silicon layer and an overlying CVD silicon oxide layer followed by oxidation which oxidizes the intermediate silicon layer to silicon oxide (see col 11, lines 60-65; col12, lines 49-53).

Thus, Ishitsuka does not disclose several aspects of Applicants disclosed and claimed invention including:

Ishitsuka fails to disclose:

"forming a plurality of stress relaxed liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;

then forming a plurality of trench filling oxide layers, said plurality selected from the group consisting of spin-on glass (SOG) and undoped silicate glass (USG);

wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to form a trench filling substantially free of stress;"

In particular, along with other aspects of Applicants disclosed and claimed invention, Ishitsuka fails to disclose **depositing a plurality of trench filling oxide layers.**

Applicants further reject Examiners apparent assertion that the isolation trench of Ishitsuka would inherently have the same stress profile as that of Applicants. Examiner has provided no support for this assertion, and as stated Ishitsuka disclose a different trench filling, e.g., formed of CVD silicon oxide or formed of silicon and an overlayer of silicon oxide, which is then anneal to form silicon oxide from the silicon layer which would create a significantly different stress profile than Applicants disclosed and claimed invention.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present

in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578,, 581 582, 212 USPQ 323, 326 (CCPA 1981).*

Tshitsuka is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. Claims 1, 2, 4, 7, 8, 12, 13, 16, 19-21 stand rejected under 35 USC 102(b) as being anticipated by Hong et al. (US

6,566,229).

Hong discloses in the background of the invention that SOG has been previously taught to fill a trench for device isolation where the SOG is treated by a plasma process which etches an upper portion of the SOG and where an HDP-CVD oxide is then used to fill a remaining portion of the trench (see col 2, lines 18-33). Hong teaches that the use of SOG is a problem because of remaining **organic** ingredients in a lower portion of the trench.

Hong overcomes the problems in the prior art by teaching depositing **polysilizane** by an **SOG method.** Hong teaches that it is preferable to **fill the trench followed by etchback** to form a recess, followed by filling the recess with a CVD USG or HDP-CVD oxide (see Abstract; col 2, lines 44 to col 3, line 15).

More particularly, Hong teaches first forming a thermal oxide to line the trench followed by formation of **a silicon nitride liner** on the thermal oxide prior to depositing the polysilizane solution (col 3, lines 53-63). Hong further teaches

a two step curing process for the polysilizane SOG including a curing process up to about 400°C and a second curing process between about 700 °C and 800 °C (col 4; lines 35-56). Hong discloses that the lower part of the cured polysilizane is less oxidized compared to the upper portion which has a lower etch rate thereby inherently including a stress. Hong then teaches **etching back the cured polysilizane** to form a recess (col 4, lines 57- col 5, lines 4). A CVD oxide is then used to fill the recess (col 5, lines 18-25).

Thus, Hong fails to disclose several aspects of Applicants disclosed and claimed invention including:

Hong fails to disclose:

"forming a plurality of stress relaxed liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;

Hong also fails to disclose:

"then forming a plurality of trench filling oxide layers, said plurality selected from the group consisting of spin-on glass (SOG) and undoped silicate glass (USG);"

Hong also fails to disclose:

"wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to form a trench filling substantially free of stress;"

Hong is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete

detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

3. Claims 1-4, 7, 8, 12, 16, 19-21, 23-25 and 28 stand rejected under 35 USC 102(e) as being anticipated by Heo et al. (US 6,683,354).

Heo discloses a process for forming a trench isolation feature including a thermal oxide layer lining the trench (on the semiconductor substrate); a silicon nitride liner on the thermal oxide; an **HTO oxide liner** on the silicon nitride liner, a first (buried) oxide layer for partially filling the trench and a second buried oxide layer for filling a remaining portion of the trench (see Abstract; col 3, lines 51-53).

Heo teaches that the first oxide layer is an SOG layer which is formed by etching back the SOG layer following **deposition and curing** (see col 4, lines 50-58). Heo teaches that the function of the HTO oxide liner protects the underlying

silicon nitride liner during etching back of the SOG layer (see col 3, lines 50-52; col 4, lines 5-12) and HDP-CVD deposition of a the upper oxide layer (second buried layer).

Thus, Heo fails to disclose several aspects of Applicants disclosed and claimed invention including:

Heo fails to disclose:

"forming a plurality of stress relaxed liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;

then forming a plurality of trench filling oxide layers, said plurality selected from the group consisting of spin-on glass (SOG) and undoped silicate glass (USG);

wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to

form a trench filling substantially free of stress;"

Among other aspects of Applicants disclosed and claimed invention, Heo fails to disclose:

1) "forming a plurality of stress relaxed liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;"

2) Heo also fails to disclose "then depositing a plurality of trench filling oxide layers";

Rather, Heo discloses forming an HTO liner on a silicon nitride liner prior to forming trench filling oxide layers.

3) Heo also fails to disclose "wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to form a trench filling substantially free of stress;"

Heo is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103(a)

1. Claims 9 an 11 stand rejected under 35 USC 103(a) as being unpatentable over Hong et al., above, and further in view of Cui (US 6, 693,050).

Applicants reiterate the comments made above with respect to Hong et al.

The fact that Cui discloses using SiH4 and O2 in an HDP-CVD oxide process, in combination with Hong et al., does not further help Examiner in establishing a *prima facie* case of obviousness.

2. Claims 1-4, 7, 9, 10, 12, 16, 19-22, and 25-28 stand rejected under 35 USC 103(a) as being unpatentable over Ahn (US 6,596,607) in view of Oyamatsu (US 6,261,920).

Ahn discloses a method of forming a trench isolation feature by forming a silicon nitride liner on either the wall of the trench or on thermal oxide layer; forming an HTO oxide on the silicon nitride liner (see col 4, lines 20-32) filling the trench with a first buried oxide layer which is disclosed to be SOG or USG (col 4, lines 27-30; col 4, lines 49-54); exposing an upper portion of the silicon nitride liner by recessing the first buried oxide layer by wet etching and then removing the exposed portion of the silicon nitride liner; and then filling the recess of the trench with a second buried oxide layer disclosed to be USG or SOG (see Abstract; col 4, lines 1-6).

Thus, Ahn does not disclose several aspects of Applicants disclosed and claimed invention:

Ahn does not disclose:

"forming a plurality of stress relaxed liner layers comprising an uppermost plurality of nitride liners selected

from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;"

Rather, Ahn discloses and teaches forming a single silicon nitride liner followed by forming an HTO oxide liner on the silicon nitride liner.

Ahn does not disclose:

"then forming a plurality of trench filling oxide layers, said plurality selected from the group consisting of spin-on glass (SOG) and undoped silicate glass (USG);

wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to form a trench filling substantially free of stress;"

Rather, Ahn discloses and teaches filling the trench with

SOG followed curing and then partial removal by etching which is also followed by removing exposed portion of the silicon nitride liner which **does not** then **line** the trench. Therefore Ahn by teaching **partial removal** of a silicon nitride liner teaches away from Applicants disclosed and claimed invention.

The fact that Oyamatsu discloses that a single layer of LPCVD silicon oxide is used to fill an isolation trench which is formed **without a liner** and where the trench is formed according to a different etching process than the process of Ahn, and also teaches that the single trench filling layer is annealed to **reduce** stress of the **LPCVD oxide** does not further help Examiner in establishing a prima facie case of obviousness with respect to Applicants disclosed and claimed invention.

There is no apparent motivation for combining the teachings of Ahn and Oyamatsu. For example, there is no suggestion in Oyamatsu that more than one buried layer (plurality of trench filling layers) may be used to fill the isolation trench and there is no suggestion that the dual trench filling layers in

Ahn **including a partially removed silicon nitride liner** would have an undesirable stress or would benefit from an annealing process. There is also no recognition of the problem or a solution to the problem found in the combined references that Applicants have recognized and solved by their disclosed and claimed invention: "A method of forming a stress relaxed shallow trench isolation (STI) structure to improve charge mobility of a MSOFET device"

Even assuming *arguendo*, a proper motivation for combining the teachings of an isolation trench with the **partially removed single silicon nitride liner layer** in the method of Ahn with the **single LPCVD trench filling oxide layer** in the method of Oyamatsu, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the

prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler,* 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

3. Claims 29-31 stand rejected under 35 USC 103(a) as being unpatentable over Heo et al., above.

Applicants reiterate the comments made above with respect to Heo et al.

Examiner appears to argue that in the method of Heo who discloses forming an SiO2/SiN/SiO2 stack of liner layers that it would be inherent that during anneal steps disclosed in Heo that "some nitrogen atoms within the SiN layer would diffuse into surrounding SiO2 layers, thus creating **various strata** of SiO2, SiN, and SiON". Applicants reject any notion of inherency and Examiner provides no support for this assertion of inherency.

Nevertheless Applicants do not claim "various strata of SiO2, SiN, and SiON", and further, such an assertion of inherency does not produce Applicants disclosed and claimed invention.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578,, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

"In relying on the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent

characteristic *necessarily* flows from the teachings of the applied prior art." *Ex Parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)*

In summary none of the cited references, either singly or in combination, discloses or suggests Applicants disclosed and claimed invention and therefore do not establish a *prima facie* case of obviousness with respect to Applicants independent claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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